REMARKS

This amendment is responsive to the Office Action dated October 22, 2004. Applicants have amended claims 1, 12, 16, 18, 29, 32, 34, 49 and 50, and added new claim 53. Claims 1-53 are pending.

Claim Rejection Under 35 U.S.C. § 102

Claims 1, 2, 4, 5, 7, 8, 10-18, 34-41, 43, 44, and 47-49

In the Office Action, the Examiner rejected claims 1, 2, 4, 5, 7, 8, 10-18, 34-41, 43, 44, and 47-49 under 35 U.S.C. 102(e) as being anticipated by Shenoi et al. (USPN 6,490,296). Applicants respectfully traverse the rejection to the extent such rejection may be considered applicable to the amended claims. Shenoi et al. fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

For example, with respect to amended claim 1, Shenoi et al. fails to teach or suggest receiving data packets from a plurality of links in one or more interface cards according to a multi-link protocol, and forwarding the data packets from the interface cards of the network device to a multi-link service card of the network device for sequencing. Similarly, with respect to claim 7, Shenoi et al. fails to teach or suggest receiving a set of fragments from a plurality of links in one or more interface cards according to a multi-link protocol, the set of fragments collectively comprising an unsequenced data packet, and sending the fragments to a multi-link service card for sequencing. With respect to claim 12, Shenoi et al. fails to teach or suggest sequencing the data blocks in a multi-link service card of a network device.

In rejecting claims 1, 7 and 12, the Examiner stated that Shenoi et al. teaches "data cells [that] undergo multi-link segmentation and reassembly via virtual circuits at a location" (emphasis added) and cited the Abstract, column 9, lines 50-54, and FIG. 8. The Examiner is correct that Shenoi et al. generally describes multi-link segmentation and reassembly. However, contrary to the Examiner's assertion, Shenoi et al. makes no mention of sequencing performed by a multi-link service card that is separate from the interface cards that receive the data packets or fragments, as required by claims 1, 7, and 12. The Abstract and FIG. 8 of Shenoi et al., cited by the Examiner, show only the general proposition that data sent over multiple links are

resequenced when received at a location. Shenoi et al. makes clear that the term "location," relied upon by the Examiner, generally refers to a computer within a network. As one example, at col. 1, ll. 38-45, Shenoi et al. states:

> *Consider, for example, an end-user that requires a Private Network linking three separate locations, A, B, and C. Assume that a 56 kbps connection is required between each pair of locations. One approach to providing this service is to have dedicated 56 kbps access links between the customer premises and the Service Provider Network (often called the "cloud"). Each location would have two such dedicated "DDS" (Digital Data Service) links (emphasis added).*

As another example, at col. 5, ll. 32-42, Shenoi et al. states:

> *Referring to FIG. 4, the notion of "Higher Layers" refers to the manner in which information (data) is handled at the application layer. For example, the source of data may be computer generated, destined as a file transfer to another location (computer); the source of data may be a telephone/PBX as in a voice call between this and another location (emphasis added).*

Consequently, Shenoi et al. fails to teach or suggest receiving data packets from a plurality of links in one or more interface cards according to a multi-link protocol, and forwarding the data packets from the interface cards of the network device to a multi-link service card of the network device for sequencing. Similarly, with respect to claim 7, Shenoi et al. fails to teach or suggest receiving a set of fragments from a plurality of links in one or more interface cards according to a multi-link protocol, the set of fragments collectively comprising an unsequenced data packet, and sending the fragments to a multi-link service card for sequencing. With respect to claim 12, Shenoi et al. fails to teach or suggest sequencing the data blocks in a multi-link service card of a network device.

Of course, the claims dependent on independent claims 1, 7, and 12, i.e., claims 2-6, 8-11, and 13-18, incorporate all of the limitations of the respective base claims, and therefore are patentable for at least the reasons expressed above.

Moreover, with respect to claims 2, 8, and 16, Shenoi et al. fails to disclose a multi-link service card that is not directly coupled to any of the links. The Examiner seems to suggest that because Shenoi et al. discusses links that are "virtual circuits," these links are therefore not associated with physical links. However, the fact that a link is a "virtual circuit" does not imply that it the element performing the sequencing is not coupled to the links. In fact, Shenoi et al. discloses that the element responsible for sequencing (multilink controller/memory write controller 1201), is coupled to the virtual circuit links. Col. 4, ll. 7-11; col. 16, ll. 7-8, 29-32.

Shenoi et al. therefore fails to teach a multi-link service card not directly coupled to any of the links, as required by claims 2, 8, and 16.

With respect to claims 5, 11, and 14, Shenoi et al. again makes no mention of a multi-link service card to perform fragmentation, separate from the interface card that initially receives the data, as required by these claims. Rather, Shenoi et al. teaches only that fragmentation is done generally at a computer (location), but again, does not disclose fragmentation performed by a multi-link service card.

With respect to claim 17, Shenoi et al. fails to disclose assembling the data blocks in a second multi-link service card. Shenoi et al. lacks any teaching of multi-link service cards, and thus does not disclose assembling data blocks in a second multi-link card, distinct from a first multi-link service card that performs sequencing.

With respect to claim 18, Shenoi et al. does not teach prioritizing the data blocks in a multi-link service card. The "prioritizing" described in Shenoi et al. is not prioritizing of data blocks in a multi-link service card, since, as discussed above, no multi-link service card is present in Shenoi et al. Further, the statement by the Examiner that "the scheduler can prioritize which virtual circuits will be serviced first" is not pertinent, since it is prioritization of data blocks, not prioritization of the plurality of links, that claim 18 requires.

With respect to independent claim 34, as amended, Shenoi et al. fails to disclose a multi-link service card for insertion within a network device. Further, Shenoi et al. fails to teach or suggest a multi-link service card having an electrical interconnection interface for coupling to the network device, and an input logic unit that receives data blocks via the electrical interconnection interface. Although Shenoi et al. may disclose receiving data cells, sequencing data cells, and transmitting the sequenced data cells, it does not disclose a multi-link service card as claimed by the Applicants by amended claim 34.

With respect to independent claim 44, the Examiner stated that Shenoi et al. discloses a method in which "sequence numbers are stored in a buffer in the order data cells were received." Applicants respectfully submit that the Examiner has misunderstood the scope and content of Shenoi et al.

Although Shenoi et al. may describe a method in which data cells are written into a buffer in the order received, col. 13, ll. 38-53, it fails to disclose "storing sequence numbers for the data

blocks in data queues in the order the data blocks were received, the data blocks received from each link being stored in a unique queue assigned to the respective link," as required by claim 44. Shenoi et al. contemplates a completely different scheme for sequencing received data, and does not provide any teaching that would have suggested the desirability of modification to include the method of claim 44.

In order to support an anticipation rejection under 35 U.S.C. 102(e), it is well established that a prior art reference must disclose each and every element of a claim. This well known rule of law is commonly referred to as the "all-elements rule."[1] If a prior art reference fails to disclose any element of a claim, then rejection under 35 U.S.C. 102(e) is improper.[2]

Shenoi et al. fails to disclose each and every limitation set forth in claims 1, 2, 4, 5, 7, 8, 10-18, 34-41, 43, 44, and 47-49. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicants' claims 1, 2, 4, 5, 7, 8, 10-18, 34-41, 43, 44, and 47-49 under 35 U.S.C. 102(e). Withdrawal of this rejection is requested.

Claims 50-51

In the Office Action, the Examiner rejected claims 50 and 51 under 35 U.S.C. § 102(b) as being anticipated by Maurya (USPN 6,160,808). Applicants respectfully submit that Maurya does not qualify as prior art under § 102(b) as it was not published more than one year before Applicants' filing date. However, Maurya may qualify under § 102(e). In any case, Applicants respectfully traverse the rejection. Maurya fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. §§ 102(b) and 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

Maurya fails to teach receiving data packets in one or more interface cards of a network device, sending the data packets to a service card of the network device for prioritization, and sending the prioritized data packets to the interface cards of the network device for communication to a destination device over a computer network, as required by claim 50. In contrast, the Examiner stated Maurya teaches that multi-link packets are received at a terminal

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[1] *See Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 231 USPQ 81 (CAFC 1986) ("[I]t is axiomatic that for prior art to anticipate under 102 it has to meet every element of the claimed invention.").
[2] *Id*; *see also Lewmar Marine, Inc. v. Barient, Inc.* 827 F.2d 744, 3 USPQ2d 1766 (CAFC 1987); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (CAFC 1990); *C.R. Bard, Inc. v. MP Systems, Inc.*, 157 F.3d 1340, 48 USPQ2d 1225 (CAFC 1998); *Oney v. Ratliff*, 182 F.3d 893, 51 USPQ2d 1697 (CAFC 1999); *Apple Computer, Inc. v. Articulate Systems, Inc.*, 234 F.3d 14, 57 USPQ2d 1057 (CAFC 2000).

adapter, with "prioritizing" also done at the same terminal adapter. Col. 15, ll. 34-38. This is directly at odds with claim 50, which requires that data packets be received in an interface card, then sent to a separate service card for prioritization.

Moreover, Applicants respectfully submit that the Examiner has misunderstood the scope and content of Maurya. The Examiner stated that "each data packet is sent to the adapter for prioritization based on their multilink header info and sequence number." However, the section cited by the Examiner teaches that the data packets are "encapsulated . . . and sequenced by that terminal adapter into an outgoing multi-link packet." Col. 15, ll. 36-38 (emphasis added). Thus, the portion of Maurya cited by the Examiner addresses what happens before packets are sent, but does not teach prioritizing data packets at a service card after they have been received, as required by claim 50.

Maurya fails to disclose each and every limitation set forth in claims 50 and 51. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicants' claims 50 and 51 under 35 U.S.C. §§102(b) and 102(e). Withdrawal of this rejection is requested.

Claims 19-26 and 29-33

In the Office Action, the Examiner rejected claims 19-26 and 29-33 under 35 U.S.C. 102(b) as being anticipated by Gai et al. (USPN 6,167,445). Applicants respectfully submit that Gai et al. does not qualify as prior art under § 102(b) because it was not published more than one year before Applicant's filing date. However, Gai et al. may qualify under § 102(e). In any case, Applicant respectfully traverses the rejection to the extent such rejection may be considered applicable to the amended claims. Gai et al. fails to disclose each and every feature of the claimed invention, as required by 35 U.S.C. §§102(b) and 102(e), and provides no teaching that would have suggested the desirability of modification to include such features.

For example, Gai et al. fails to teach or suggest "[a] router comprising a plurality of cards, wherein the cards include a first card for receiving data blocks from a computer network and a second card for sequencing the data blocks," as recited by Applicants' amended claim 29. Moreover, Gai et al. fails to teach or suggest "a routing control unit coupled to the interface card and the multi-link service card to forward the set of data blocks to the multi-link service card for sequencing," as recited by Applicants' claim 19.

The Examiner stated Gai et al. teaches routers that "inherently contain interface cards for receiving data packets and furthermore possess sequencing/reassembly capabilities." This, however, does not meet the requirement of claims 19 and 29 that the card for receiving and the card for sequencing are separate and distinct. Gai et al. fails to teach or suggest a router having a multi-link service card for sequencing data blocks that is distinct from the interface card that receives the data blocks, as required by claim 19. Moreover, Gai et al. fails to teach or suggest a routing control unit coupled to the interface card and the multi-link service card to forward the set of data blocks to the multi-link service card for sequencing, as required by claim 19.

Rather, Gai et al. only states generally that "routers . . . are computers having transmitting and receiving circuitry and components, including network interface cards (NICs) establishing physical ports, for exchanging data frames." Col. 8, ln. 67–col. 9, ln. 3.

Gai et al. fails to disclose each and every limitation set forth in claims 19-26 and 29-33. For at least these reasons, the Examiner has failed to establish a prima facie case for anticipation of Applicants' claims 19-26 and 29-33 under 35 U.S.C. §§102(b) and 102(e). Withdrawal of this rejection is requested.

Claim Rejection Under 35 U.S.C. § 103

Claims 3, 9, 27, 28, 45 and 46

In the Office Action, the Examiner rejected claims 3, 9, 27, 28, 45 and 46 under 35 U.S.C. 103(a) as being unpatentable over Shenoi et al. in view of Gai et al. Applicants respectfully traverse the rejection. The applied references fail to disclose or suggest the inventions defined by Applicants' claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

In regard to claims 3 and 9, the Examiner correctly recognized that Shenoi et al. fails to teach the method of claim 3, wherein the multi-link service card is integrated with one of the network cards. The Examiner asserted that it would have been obvious to modify the Shenoi system in view of the teachings of Gai et al. Specifically, the Examiner stated that Gai et al. teaches "a routing system comprising a coupling or an integration between multi-link service and network interfaces." However, Gai et al. fails to teach a multi-link service card for sequencing data packets at all, let alone a multi-link service card integrated with an interface card that

receives data packets. Thus, modifying Shenoi et al. in view of Gai et al. fails to achieve Applicants' invention, as required by claims 3 and 9.

With respect to claim 27, the Examiner correctly recognized that Gai et al. fails to disclose a plurality of multi-link service cards. The Examiner stated that Shenoi et al. teaches data transmitted according to a multilink protocol, and that it would have been obvious to modify the Gai system in view of Shenoi et al. However, as discussed above, neither Shenoi et al. nor Gai et al. discloses a multi-link service card distinct from an interface card, let alone a plurality of multi-link service cards. Thus, modification of the Gai system in view of Shenoi fails to achieve Applicants' invention, as required by claim 27. Moreover, the Examiner states the motivation for the modification is "for the purposes of load-balancing and extending the services of the system." None of the cited references provide such motivation, as is required. Applicant requests the Examiner identify support for the motivation

In regard to claim 28, the Examiner correctly recognized that Gai et al. fails to teach a router wherein the routing control unit forwards sequenced data blocks to the multi-link service card for fragmentation. The Examiner endeavored to fill this gap by adding the teachings of Shenoi et al. As discussed above with respect to claim 5, however, Shenoi et al. fails to disclose a multi-link service card that fragments data, let alone a routing control unit that forwards sequenced data blocks to the multi-link service card for fragmentation. Therefore, the modification of Gai et al. and Shenoi et al. does not yield forwarding sequenced data blocks to a multi-link service card for fragmentation, as required by claim 28. Moreover, the Examiner states the motivation for the modification is "for the purposes of providing fragmentation at an individual interface in communication with the routing system." None of the cited references provide such motivation, as is required. Applicant requests the Examiner identify support for the motivation.

Claims 6 and 42

In the Office Action, the Examiner rejected claims 6 and 42 under 35 U.S.C. 103(a) as being unpatentable over Shenoi et al. in view of Maurya. Applicants respectfully traverse the rejection. The applied references fail to disclose or suggest the inventions defined by Applicants' claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed invention.

The Examiner correctly recognized that Shenoi et al. fails to teach prioritizing the sequenced data packets to provide quality of service. The Examiner proposed to supplement Shenoi et al. with the teachings of Maurya. The Examiner stated that Maurya teaches prioritizing data packets according to their sequence numbers. However, Maurya makes no mention of quality of service. Thus, modification of the Shenoi system does not achieve Applicants' claimed invention, including prioritizing the sequenced data packets to provide quality of service, as required by claims 6 and 42.

Claims 3, 6, 9, 27, 28, 42, 45, 46, and 52 are dependent on the independent claims discussed above with respect to 35 U.S.C. 102, and are patentable for the same reasons. For at least these reasons, the Examiner has failed to establish a prima facie case for non-patentability of Applicants' claims 3, 6, 9, 27, 28, 42, 45, 46, and 52 under 35 U.S.C. 103(a). Withdrawal of this rejection is requested.

New Claims:

Applicants have added claim 53 to the pending application. The applied references fail to disclose or suggest the inventions defined by Applicants' new claims, and provide no teaching that would have suggested the desirability of modification to arrive at the claimed inventions. As one example, the references fail to disclose or suggest an interface card and a multi-link service card that comprise removable cards that may be inserted and removed from a network device, as recited by claim 53. No new matter has been added by the new claim.

CONCLUSION

All claims in this application are in condition for allowance. Applicants respectfully request reconsideration and prompt allowance of all pending claims. Please charge any additional fees or credit any overpayment to deposit account number 50-1778. The Examiner is invited to telephone the below-signed attorney to discuss this application.

Date: January 21, 2005

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